

DEPARTMENT OF COMPUTER SYSTEM ENGINEERING Digital Integrated Circuits - ENCS333

Dr. Khader Mohammad Lecture #14

Clock Distribution

Digital Integrated Circuits

	Course topics and Schedule
	Subject
	Introduction to Digital Integrated Circuits Design
2	Semiconductor material: pn-junction, NMOS, PMOS
3	IC Manufacturing and Design Metrics CMOS
4	Transistor Devices and Logic Design
	The CMOS inverter
5	Combinational logic structures
6	Layout of an Inverter and basic gates
	Static CMOS Logic
8	Dynamic Logic
9	Sequential logic gates; Latches and Flip-Flops
10	Summary : Device modeling parameterization from I-V curves.
	Interconnect: R, L and C - Wire modeling
	Parasitic Capacitance Estimation
	Timing
14	Power dissipation;
	Clock Distribution
16	Arithmetic building blocks
	Memories and array structures
	Final & Project discussion

Clock Distribution Tree



Phase Locked Loop (PLL)



 PLLs produce an on-chip core clock at a multiple of the off-chip system clock.

PLL Overview

- PLLs
 - Typically there are two PLLs on a chip
 - IOPLL and COREPLL
 - IOPLL gets an external "xxbclk" and generates the address clock (2x) and data clock (4x)
 - These clocks are only used in the PADs
 - COREPLL takes the IOPLL output as reference and generates the core clock for entire chip



Global Clock Buffer



 Global clock buffers can use variable delay to compensate for RC mismatches across a die

Local Clock Buffers (LCBs)



- Local Clock Buffers Support:
 - Clock gating for power reduction
 - Intentional clock skew insertion for timing optimization

Clock Skew



 A single transition of the core clock does not arrive at all sequentials at the same time.



Clock Jitter



Variations of tree distribution networks



Tree





X-Tree



H-Tree



Tapered H-Tree